WHAT IS CLAIMED IS:

1. A graphic computing apparatus comprising:

a shape divider which divide a unit shape of a surface of an object present in a three-dimensional space into a plurality of subpolygons arranged two-dimensionally and having an arbitrary size, to generate a subpolygon mesh;

a vertex processor which computes parameters required for drawing in units of pixels with respect to subpolygons for each vertex of the subpolygon mesh generated by said shape divider;

a rendering processor which computes drawing data in units of pixels on the basis of the parameters computed by said vertex processor and picture data for texture mapping; and

a frame memory which stores the drawing data as picture data together with at least data for texture mapping required for said rendering processor to compute the drawing data.

2. An apparatus according to claim 1, further comprising a frame memory readout route configured to read out at least the data for texture mapping from said frame memory, and transfer the readout data to said vertex processor, and

wherein said vertex processor reads at least the data for texture mapping corresponding to each vertex of the subpolygon mesh from said frame memory via said

frame memory readout route, and computes the parameters required for drawing in units of pixels of the subpolygons for each vertex of the subpolygon meshes using the read data.

3. An apparatus according to claim 2, further comprising a cache configured to temporarily store the data read via said frame memory readout route.

4. An apparatus according to claim 1, wherein said vertex processor has a plurality of processing elements which respectively perform arithmetic operations for computing the parameters required for drawing in units of pixels of the subpolygons for each vertex of the subpolygon mesh, and simultaneously makes the arithmetic operations for a plurality of vertexes in accordance with an identical program.

5. An apparatus according to claim 4, wherein said plurality of processing elements repeat the process for simultaneously making the arithmetic operations for each row of the subpolygon mesh in correspondence with the number of rows of the subpolygon mesh.

6. An apparatus according to claim 4, wherein said plurality of processing elements are linearly arranged and have data transfer routes for connecting the processing elements neighboring in an arrangement direction, and all the processing elements simultaneously transfer at least some of internal data to the

processing elements neighboring in the arrangement direction via the data transfer routes.

7. An apparatus according to claim 6, further comprising a triangle construction unit which constructs the arithmetic operation results of said plurality of processing elements into a consecutive triangle strip, and transfers the triangle strip to said rendering processor.

8. An apparatus according to claim 1, wherein said rendering processor computes the drawing data using mapping in units of vertexes and mapping in units of pixels together.

9. A graphic computing apparatus comprising:

a shape divider which divides a unit shape of a surface of an object present in a three-dimensional space into a plurality of subpolygons which are arranged two-dimensionally and have an arbitrary size, to generate a subpolygon mesh;

a plurality of vertex processors which compute parameters required for drawing in units of pixels with respect to subpolygons for each vertex of the subpolygon mesh generated by said shape divider;

an exchanger which arbitrarily exchanges and connects an output of said shape divider and inputs of said plurality of vertex processors;

a rendering processor which computes drawing data in units of pixels on the basis of the parameters

computed by said vertex processors and picture data for texture mapping; and

a frame memory which stores the drawing data as picture data together with at least data for texture mapping required for said rendering processor to compute the drawing data.

10. An apparatus according to claim 1, further comprising a frame memory readout route configured to read out at least the data for texture mapping from said frame memory, and transfer the readout data to said vertex processor, and

wherein said vertex processor reads at least the data for texture mapping corresponding to each vertex of the generated subpolygon mesh from said frame memory via said frame memory readout route, and computes the parameters required for drawing in units of pixels of the subpolygons for each vertex of the subpolygon meshes using the read data.

11. An apparatus according to claim 10, further comprising a cache configured to temporarily store the data read via said frame memory readout route.

12. An apparatus according to claim 9, wherein said vertex processor has a plurality of processing elements which respectively perform arithmetic operations for computing the parameters required for drawing in units of pixels of the subpolygons for each vertex of the subpolygon mesh, and simultaneously makes

the arithmetic operations for a plurality of vertexes in accordance with an identical program.

13. An apparatus according to claim 12, wherein said plurality of processing elements repeat the process for simultaneously making the arithmetic operations for each row of the subpolygon mesh in correspondence with the number of rows of the subpolygon mesh.

14. An apparatus according to claim 12, wherein said plurality of processing elements are linearly arranged and have data transfer routes for connecting the processing elements neighboring in an arrangement direction, and all the processing elements simultaneously transfer at least some of internal data to the processing elements neighboring in the arrangement direction via the data transfer routes.

15. An apparatus according to claim 12, further comprising a triangle construction unit which constructs the arithmetic operation results of said plurality of processing elements into a consecutive triangle strip, and transfers the triangle strip to said rendering processor.

16. An apparatus according to claim 9, wherein said rendering processor computes the drawing data using mapping in units of vertexes and mapping in units of pixels together.

17. A graphic computing apparatus comprising:

a plurality of shape dividers each of which divides a unit shape of a surface of an object present in a three-dimensional space into a plurality of subpolygons which are arranged two-dimensionally and have an arbitrary size, to generate a subpolygon mesh;

an input distributor which distributes data of the unit shape to said plurality of shape dividers;

a plurality of vertex processors each of which computes parameters required for drawing in units of pixels with respect to subpolygons for each vertex of the subpolygon mesh generated by said shape divider;

an exchanger which arbitrarily exchanges and connects outputs of said plurality of shape dividers and inputs of said plurality of vertex processors;

a rendering processor which computes drawing data in units of pixels on the basis of the parameters computed by said vertex processors and picture data for texture mapping; and

a frame memory which stores the drawing data as picture data together with at least data for texture mapping required for said rendering processor to compute the drawing data.

18. An apparatus according to claim 17, further comprising a frame memory readout route configured to read out at least the data for texture mapping from said frame memory, and transfer the readout data to said vertex processor, and

wherein said vertex processor reads at least the data for texture mapping corresponding to each vertex of the subpolygon mesh from said frame memory via said frame memory readout route, and computes the parameters required for drawing in units of pixels of the subpolygons for each vertex of the subpolygon meshes using the read data.

19. An apparatus according to claim 18, further comprising a cache configured to temporarily store the data read via said frame memory readout route.

20. An apparatus according to claim 17, wherein said vertex processor has a plurality of processing elements which respectively perform arithmetic operations for computing the parameters required for drawing in units of pixels of the subpolygons for each vertex of the subpolygon mesh, and simultaneously makes the arithmetic operations for a plurality of vertexes in accordance with an identical program.

21. An apparatus according to claim 20, wherein said plurality of processing elements repeat the process for simultaneously making the arithmetic operations for each row of the subpolygon mesh in correspondence with the number of rows of the subpolygon mesh.

22. An apparatus according to claim 20, wherein said plurality of processing elements are linearly arranged and have data transfer routes for connecting

the processing elements neighboring in an arrangement direction, and all the processing elements simultaneously transfer at least some of internal data to the processing elements neighboring in the arrangement direction via the data transfer routes.

23. An apparatus according to claim 20, further comprising a triangle construction unit which constructs the arithmetic operation results of said plurality of processing elements into a consecutive triangle strip, and transfers the triangle strip to said rendering processor.

24. An apparatus according to claim 17, wherein said plurality of shape dividers share a program memory configured to store a processing program.

25. An apparatus according to claim 17, wherein said rendering processor computes the drawing data using mapping in units of vertexes and mapping in units of pixels together.